Claims 19, 21, 23, and 26 have been rejected under 35 USC 112(2) as being indefinite. The claims have been amended in the manner suggested by the examiner. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 19, 21, 23 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent 5,635,847 ("Seidel") in view of U.S. patent 5,483,421 ("Gedney") and further in view of U.S. patent 5,680,936 ("Beers"). Applicants respectfully traverse this rejection in view of the amended claims for the following reasons, each of which is an independent reason that is individually sufficient to justify allowance of the claims:

1) Independent claim 19 recites coupling cache memory devices to the interposer, and coupling a microprocessor to the substrate that is coupled to the interposer. None of the cited references disclose or suggest coupling a microprocessor and cache memory devices in the claimed manner.

2) Independent claim 19 recites testing multiple cache memory devices on a multi-chip subassembly with at least one passive component, then coupling the subassembly to a substrate if the test passes. Neither Gedney nor Beers discloses or suggests any kind of assembly process that is conditioned on test results. Gedney does not discuss the subject of testing at all, while Beers separates tested printed circuit boards into those that passed the testing and those that did not, but does nothing further with the boards. Seidel discloses testing the connections on a substrate (column 1 lines 31, 34, 64), or burning in semiconductor chips (column 1 line 65, column 2 line 50) but does not disclose or suggest testing cache memory devices on the substrate (emphasis provided).

3) Independent claim 19 recites soldering the cache memory subassembly to a substrate and coupling a processor device to the substrate. At most, the printed circuit boards of Beers might be plugged into the connectors on a motherboard (something that might be suggested in other references but is not suggested by Beers and Gedney), but would not be soldered to a substrate having other integrated circuits on it. Seidel does not disclose or suggest the use of a cache memory subassembly or the use of a microprocessor device.

4) Beers tests a completed printed circuit board. At most, the printed circuit board of Beers would contain multi-chip subassemblies that had already been attached to the printed circuit board before Beers begins testing, which is contrary to the claims and which represents the problematic prior art approach that Applicant's invention is intended to overcome.

Claims 21-26 depend from claim 19 and therefore contain the same limitations not disclosed or suggested by the cited references. Claims 22, 24 and 25 are not currently under consideration, but will be similarly amended for consistent terminology as necessary once the other pending claims have been allowed.

CONCLUSION

For the aforementioned reasons, Applicants maintain that claims 19, 21, 23 and 26 are now in condition for allowance. Applicants further maintain that since generic claim 19 is in condition for allowance, claims 22, 24 and 25 should now be considered by

the Examiner. No fee is believed due with this response. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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APPENDIX A

MARKED-UP COPY OF AMENDED CLAIMS

19. (Amended five times) A method of assembling a multi-chip device comprising:

providing an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of selected ones of the plurality of conductive pads;

coupling a plurality of [semiconductor dice] cache memory devices and at least one passive device to the first surface to form a multi-chip subassembly, wherein the at least one passive device is selected from a group [comprising] consisting of resistors, capacitors, and inductors;

testing said plurality of [semiconductor dice] cache memory devices on said interposer;

coupling said interposer to a substrate with the solder balls after said testing if said plurality of [semiconductor dice passes] cache memory devices pass said testing; and

coupling [at least one other semiconductor] a microprocessor device to the substrate.

21. (Amended three times) The method of claim 19 wherein [providing] the interposer comprises [providing the interposer having] organic material.

23. (Amended four times) The method of claim 19 further comprising not coupling said interposer to the substrate if said plurality of [semiconductor dice] cache memory devices does not pass said testing.